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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 10/625,068
Filing Date ..... July 22, 2003
Inventor ..... Arup Bhattacharyya
Assignee ..... Micron Technology, Inc.
Group Art Unit 2824
Examiner ..... Christian D. Wilson
Attorney Docket No. MI22-2362
Title: Methods of Making Semiconductor-on-Insulator Thin Film Transistor Constructions

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Although it is believed that no fees are due, the Commissioner is hereby authorized to charge any fees under 37 C.F.R. 1.16 and 1.17 which may be required by this paper to Deposit Account No. 23-0925.

Dated: 1/27/05 By:
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Confirmation No. 8254
Filing Date ..... July 22, 2003
Inventor ..... Arup Bhattacharyya
Assignee ..... Micron Technology, Inc.
Group Art Unit 2824
Examiner ..... Christian D. Wilson
Attorney's Docket No. MI22-2362
Customer No. 021567
Title: Methods of Making Semiconductor-on-Insulator Thin Film Transistor Constructions

RESPONSE TO NOVEMBER 29, 2004 OFFICE ACTION

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: David G. Latwesen (Tel. 509-624-4276; Fax 509-838-3424)
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AMENDMENTS

In the Specification

No changes.

In the Claims

Claims 1-61 (canceled).

Claim 62 (original): A process of forming a semiconductor-on-insulator construction, comprising:

forming a first layer over a substrate, the first layer being electrically insulative;

forming a plurality of discrete islands of material over the first layer;

forming crystals in the material of the discrete islands;

forming a second layer over the discrete islands, the second layer comprising silicon and germanium;

forming metal in physical contact with the second layer; and

utilizing the metal for metal-induced-lateral-recrystallization of the second layer, the metal-induced-lateral-recrystallization converting the second layer to a crystalline material.

Claim 63 (original): The method of claim 62 wherein the crystalline material consists of a single crystal.

Claim 64 (original): The method of claim 62 wherein the crystalline material is polycrystalline.

Claim 65 (original): The method of claim 62 further comprising removing the metal from over the crystalline material.

Claim 66 (original): The method of claim 62 wherein the substrate comprises one or more of glass, semiconductive material, metal, plastic, SiO_2 and Al_2O_3.

Claim 67 (original): The method of claim 62 wherein the first layer consists of silicon dioxide.

Claim 68 (original): The method of claim 62 wherein the material of the discrete islands consists of silicon or doped silicon.

Claim 69 (original): The method of claim 62 wherein the material of the discrete islands consists of doped silicon in which the dopant concentration is from about 10^{14} atoms/cm^3 to about 10^{20} atoms/cm^3.

Claim 70 (original): The method of claim 62 wherein the discrete islands have a thickness of from about 5 nanometers to about 10 nanometers.

Claim 71 (original): The method of claim 62 wherein the second layer consists of silicon and germanium.

Claim 72 (original): The method of claim 62 wherein the second layer consists of silicon, germanium and one or more dopants.

Claim 73 (original): The method of claim 62 wherein the second layer has a thickness of from about 50 nanometers to about 100 nanometers.

Claim 74 (original): The method of claim 62 wherein the metal comprises nickel.

Claim 75 (original): The method of claim 62 wherein the forming the crystals in the material of the discrete islands comprises implanting helium into said material to form voids and subsequently exposing said material to laser-emitted electromagnetic radiation to form the crystals.

Claim 76 (original): The method of claim 75 further comprising forming a cap over the discrete islands prior to implanting the helium, and removing the cap prior to forming the second layer.

Claim 77 (original): The method of claim 76 wherein the cap comprises silicon dioxide.

Claim 78 (original): The method of claim 62 further comprising converting at least a portion of one or more of the islands to silicon dioxide after forming the second layer and prior to the metal-induced-lateral-recrystallization.

Claim 79 (original): The method of claim 78 wherein the converting comprises implanting O_2 into said one or more of the islands.

Claim 80 (original): The method of claim 62 further comprising:

forming a third layer over the second layer;

removing portions of the third layer to form openings extending through the third layer to the second layer; and

forming the metal within the openings.

Claim 81 (original): The method of claim 80 wherein the third layer comprises silicon dioxide.

Claim 82 (previously presented): A process of forming a transistor associated with a semiconductor-on-insulator construction, comprising:

forming a first layer over a substrate, the first layer being electrically insulative;

forming a plurality of discrete islands of material over the first layer;

exposing the material of the discrete islands to helium and laser-emitted electromagnetic radiation;

forming a second layer over the discrete islands, the second layer comprising silicon and germanium;

forming metal in physical contact with the second layer and utilizing the metal for metal-induced-lateral-recrystallization of the second layer, the metal-induced-lateral-recrystallization converting the second layer to a crystalline material;

forming a transistor gate over the crystalline material; and

forming a pair of source/drain regions gatedly connected to one another by the gate and extending into the crystalline material.

Claim 83 (original): The method of claim 82 wherein the forming the source/drain regions comprises implanting dopant into the crystalline material.

Claim 84 (original): The method of claim 82 wherein the crystalline material has a relaxed crystalline lattice, and further comprising:

forming a strained crystalline lattice over the relaxed crystalline lattice; and

forming the transistor gate over the strained crystalline lattice.

Claim 85 (original): The method of claim 84 wherein the strained crystalline lattice and relaxed crystalline lattice together define a crystalline mass having a thickness of less than or equal to 2000Å.

Claim 86 (original): The method of claim 84 wherein the strained crystalline lattice includes silicon.

Claim 87 (original): The method of claim 84 wherein the strained crystalline lattice includes silicon and germanium.

Claim 88 (original): The method of claim 82 wherein the transistor gate and source/drain regions are comprised by an NFET device.

Claim 89 (original): The method of claim 82 wherein the transistor gate and source/drain regions are comprised by a PFET device.

Claim 90 (original): The method of claim 82 wherein the transistor gate and source/drain regions are associated with an active region which extends into the crystalline material, and wherein an entirety of the active region within the crystalline material is within only a single crystal of the crystalline material.

Claims 91-101 (cancelled).

REMARKS

Claims 1-61 and 91-101 are cancelled, leaving claims 62-90 pending in the application. Claim 62-90 are allowed, and Applicant therefore respectfully requests that the Examiner's next action be a Notice of Allowance.

Respectfully submitted,

Dated: 1/27/05 By: _____

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